REMARKS

Claims 1- 20 are pending in the present application.

Claims 1 - 20 were rejected.

Claims 1, 9 and 17 were amended.

Claims 3 and 11 were cancelled.

Reconsideration of the claims is respectfully requested.

In Section 1 of the November 16, 2004 Office Action, the Examiner rejected Claims 1-3, 9-11 and 17 under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 5,889,816 to *Agrawal et al.* (hereafter, "*Agrawal*") in view of United States Patent No. 6,006,340 to *O'Connell* (hereafter, "*O'Connell*"). In Section 2 of the November 16, 2004 Office Action, the Examiner rejected Claims 6-8, 14-16 and 18-20 as unpatentable over *Agrawal* in view of *O'Connell* in further view of United States Patent No. 5,995,831 to *Gulliford et al.* (hereafter, "*Gulliford*"). In Section 3 of the November 16, 2004 Office Action, the Examiner rejected Claims 4, 5, 12 and 13 as unpatentable over *Agrawal* in view of *O'Connell* in further view of United States Patent No. 6,308,080 to *Burt et al.* (hereafter, "*Burt*"). The Applicant respectfully traverses these rejections.

The Applicant respectfully directs the Examiner's attention to amended independent Claim 1, which contains the unique and novel limitations herein emphasized:

> 1. (Currently Amended) For use in a base station of a wireless network, a call control processor comprising:
> a first state machine capable of performing a call processing task in response to receipt of a message retrieved from an operating system queue associated with said first state machine, said first state machine comprising an internal queue capable of

> storing a plurality of events associated with said call processing task, each of said plurality of events operable to cause said first state machine to perform a selected action, wherein said first state machine is capable of communicating with a second state machine of said call control processor by storing at least one event directly into an internal queue associated with said second state machine.

The Applicant respectfully submits that the above-emphasized limitations are not disclosed, suggested, or even hinted at in any one of the *Agrawal*, *O'Connell*, *Gulliford*, and *Burt* references individually, or in any combination of two or more of the *Agrawal*, *O'Connell*, *Gulliford* and *Burt* references.

In the November 16, 2004 Office Action, the Examiner asserted that the *Agrawal* reference describes a call control processor implemented as software on a base station CPU and cited column 7, lines 64-66 of the *Agrawal* reference in support of this assertion. Further, the Examiner asserted that the *Agrawal* reference teaches first and second state machines that communicate using queues and cited Figure 6 and column 8, lines 11-32 of the *Agrawal* reference in support of this assertion. The cited passage at column 8, lines 11-32 states:

> The organization of the software embedded on the wireless adapter is shown in FIG. 6. The software is organized as a multi-threaded system. The finite state machines corresponding to the Medium Access Control protocol at each radio port are implemented as FSMs 94 running in the interrupt mode. There is one such FSM 94 for each radio port. These can be viewed as very high priority threads. The Medium Access Control FSMs 94 communicate with a main thread 96 that runs in the user mode and handles queue management and dispatching of ATM cells to the Medium Access Control FSMs 94 on one side, and to other threads or to the base station/mobile unit CPU on the other side. The inter-thread communication is done using queues of pointers 98, with the ATM cells themselves being stored in a shared memory area. It is worth pointing out that in the case of dumb terminals with no CPU of their own, the ATM connection manager 100 and the threads that source or sink ATM cells are also run on the embedded CPU (an ARM610 processor) on the

> wireless adapter. An IRQ Handler 102 processes interrupt requests in response to a queue status change. (*emphasis added*)

Thus, the Examiner asserted that the *Agrawal* reference describes first and second state machines, implemented as software on a base station CPU, that communicate with each other via operating system queues and an operating system thread on the CPU that handles queue management. The Applicant can find no teaching in the *Agrawal* reference regarding internal queues in the state machines capable of storing events associated with a call processing task, as recited in independent Claim 1.

The Examiner acknowledged that the *Agrawal* reference lacks a teaching of a first state machine storing events directly into the queue of a second state machine. However, the Examiner also asserted that such a teaching can be found in the *O'Connell* reference. The Applicant respectfully asserts that the *O'Connell* reference describes a register file for providing an asynchronous transfer of information for a transaction from a write side domain to a read side domain. *See O'Connell, col. 3, lines 10-15.* The write side domain is so called because it writes transaction parameters to the register file, and the read side domain is so called because it reads transaction parameters from the register file. *See O'Connell, col. 2, line 66, through col. 3, line 6.* A first state machine, operating in the write side clock domain, generates transaction requests and writes them to the register file, and a second state machine, operating in the read side clock domain, reads the requests from the register file. *See O'Connell, col. 3, lines 52-66.*

Thus, the *O'Connell* reference describes an interface between finite state machines, operating at different clock speeds, employing a single, unidirectional register file. As such, the *O'Connell* reference does not describe a first state machine communicating with a second state machine by storing an event directly into an internal queue associated with the second state machine, as recited in amended independent Claim 1. Moreover, the *Gulliford* reference and the *Burt* reference fail to overcome the shortcomings of the *Agrawal* reference and the *O'Connell* reference with respect to Claim 1.

In the November 16, 2004 Office Action, the Examiner asserted that a person of ordinary skill in the art would have modified the system of the *Agrawal* reference by the teaching of the *O'Connell* reference "in order to make data transfer as efficient as possible," citing the *O'Connell* reference especially at column 1, lines 50-56. The cited passage states:

> Additionally, because getting on and off the PCI bus in order to facilitate a data transfer is very time consuming, it is desired that any data transfer be as efficient as possible. This is a particular problem for data transferred from a write side clock domain to a read side clock domain (the PCI bus), because the handshake acknowledge signals must be communicated back and forth between these two clock domains.

The teaching of the cited passage, indeed the teaching of the entire *O'Connell* reference, is a unidirectional register file used as an interface between different clock domains. The *Agrawal* reference, on the other hand, describes a system in which a plurality of state machines operating on a base station CPU communicate using queues managed by the operating system of the CPU. The Applicant respectfully asserts that there is thus no suggestion or motivation, either in the references

themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the system of the *Agrawal* reference by the interface of the *O'Connell* reference, or to combine the teachings of the two references.

The Applicant respectfully asserts that the Examiner has inappropriately applied hindsight when combining the teachings of the *Agrawal* reference and the *O'Connell* reference in order to arrive at the claimed invention recited in independent Claim 1. The teaching of a first state machine capable of performing a call processing task in response to a message retrieved from an operating system queue, having an internal queue for events associated with the call processing task, and communicating with a second state machine by storing an event directly into an internal queue associated with the second state machine comes from the Applicant's patent application.

Moreover, even if the system of the *Agrawal* reference was modified by the teaching of the *O'Connell* reference, the combination would not result in the invention as recited in amended independent Claim 1. Because the *Agrawal* system teaches a plurality of state machines, each with a single operating system queue, a person of skill in the art would apply the teaching of the *O'Connell* reference to allow a first state machine to communicate with a second state machine by writing information directly into the operating system queue of the second state machine. The combination of the *Agrawal* and *O'Connell* references would not result in a first state machine having an operating system queue and an internal queue of events and communicating with a second state machine by storing events directly into an internal queue of the second state machine, as recited in amended independent Claim 1.

For these reasons, amended independent Claim 1 recites unique and non-obvious limitations that are not disclosed, suggested or even hinted at in the *Agrawal* reference, the *O'Connell* reference, the *Gulliford* reference, and the *Burt* reference, or in any combination of two or more of the *Agrawal*, *O'Connell*, *Gulliford* and *Burt* references. This being the case, Claim 1 is patentable over the cited prior art references. Also, amended independent Claims 9 and 17 recite limitations that are analogous to the unique and non-obvious limitations recited in independent Claim 1. This being the case, independent Claims 9 and 17 also are patentable over the *Agrawal* reference, the *O'Connell* reference, the *Gulliford* reference, and the *Burt* reference, or any combination thereof.

Finally, dependent Claims 2 and 4-8, which depend from independent Claim 1, dependent Claims 10 and 12-16, which depend from Claim 9, and dependent Claims 18-20, which depend from Claim 17, contain all of the unique and non-obvious limitation of their respective base claims. This being the case, Claims 2, 4-8, 10, 12-16 and 18-20 are patentable over the *Agrawal* reference, the *O'Connell* reference, the *Gulliford* reference, and the *Burt* reference, or in any combination of two or more of the *Agrawal*, *O'Connell*, *Gulliford* and *Burt* references.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***jmockler@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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